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	Application No.	Applicant(s)	$\langle \Omega M \rangle$
Nation of Allowability	10/647,060	MEARS ET AL.	(g)
Notice of Allowability	Examiner	Art Unit	
	Thinh T. Nguyen	2818	<u></u>
The MAILING DATE of this communication and All claims being allowable, PROSECUTION ON THE MERITS herewith (or previously mailed), a Notice of Allowance (PTOLNOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT of the Office or upon petition by the applicant. See 37 CFR 1.	IS (OR REMAINS) CLOSED in 85) or other appropriate communic RIGHTS. This application is s	nthis application. If not includuring the interior in the interior will be mailed in due	ed course. THIS
1. \boxtimes This communication is responsive to <u>5/3/2005</u> .			
2. ☑ The allowed claim(s) is/are <u>1-71</u> .			
3. $igotimes$ The drawings filed on <u>22 August 2003</u> are accepted by	the Examiner.		
 4. Acknowledgment is made of a claim for foreign priority a) All b) Some* c) None of the: 1. Certified copies of the priority documents h 2. Certified copies of the priority documents h 3. Copies of the certified copies of the priority International Bureau (PCT Rule 17.2(a)). * Certified copies not received: 	ave been received. ave been received in Applicatio	n No	ition from the
Applicant has THREE MONTHS FROM THE "MAILING DAT noted below. Failure to timely comply will result in ABANDO THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		a reply complying with the re	quirements
5. A SUBSTITUTE OATH OR DECLARATION must be su INFORMAL PATENT APPLICATION (PTO-152) which			NOTICE OF
6. CORRECTED DRAWINGS (as "replacement sheets") r	nust be submitted.		
(a) including changes required by the Notice of Draftsp	person's Patent Drawing Review	v (PTO-948) attached	
1) 🔲 hereto or 2) 🔲 to Paper No./Mail Date	<u></u> .		
(b) ☐ including changes required by the attached Examir Paper No./Mail Date	ner's Amendment / Comment or	in the Office action of	,
Identifying indicia such as the application number (see 37 CF each sheet. Replacement sheet(s) should be labeled as such			e back) of
 DEPOSIT OF and/or INFORMATION about the de attached Examiner's comment regarding REQUIREMENT 	PPOSIT OF BIOLOGICAL MATE NT FOR THE DEPOSIT OF BIO	ERIAL must be submitted. DLOGICAL MATERIAL.	Note the
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Attachment(s) 1. ☐ Notice of References Cited (PTO-892)	5. ☐ Notice of In	formal Patent Application (PT	O-152)
2. 🔲 Notice of Draftperson's Patent Drawing Review (PTO-94		ummary (PTO-413),	
 Information Disclosure Statements (PTO-1449 or PTO/S Paper No./Mail Date 		Mail Date Amendment/Comment	
4. Examiner's Comment Regarding Requirement for Depos	8. Examiner's	Statement of Reasons for Allo	owance
of Biological Material	9. 🗌 Other	→	
กรับ	id Nelms		
Supervisory	Patent Examiner		
technolog	y Center 2800		

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DETAILED ACTION

Reason for allowance

1. Claims 1-71 are allowed. The following is an examiner's statement of reason for allowance:

I/ Group I: Claims 1-20:

None of the references of record teaches or suggests the claimed

SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE
having the limitations:

--" each group of layers of said superlattice comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon;

said energy-band modifying layer comprising at least one nonsemiconductor monolayer constrained within a crystal lattice of adjacent base
semiconductor portions so that said superlattice has a higher charge carrier
mobility in the parallel direction than would otherwise be present. "--

and all other limitations as recited in claim 1.

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II/ Group II: Claims 21-34:

None of the references of record teaches or suggests the claimed

SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE

having the limitations:

--" each group of layers of said superlattice comprising a plurality of stacked

silicon monolayers defining a silicon portion and an energy band-modifying layer

thereon; said energy-band modifying layer comprising at least one oxygen

monolayer constrained within a crystal lattice of adjacent silicon portions so that

said superlattice has a higher charge carrier mobility in the parallel direction than

would otherwise be present. "--

and all other limitations as recited in claim 21.

III/ Group III: Claims 35-45:

None of the references of record teaches or suggests the claimed

SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE

having the limitations:

--" each group of layers of said superlattice comprising less than eight

stacked base semiconductor monolayers defining a base semiconductor portion

and an energy band-modifying layer thereon; said energy-band modifying layer

comprising a single non-semiconductor monolayer constrained within a crystal

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lattice of adjacent base semiconductor portions so that said superlattice has a higher charge carrier mobility in the parallel direction than would otherwise be

present. "--

and all other limitations as recited in claim 35.

IV/ Group IV: Claims 46-52:

None of the references of record teaches or suggests the claimed

SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE

having the limitations:

--" regions for causing transport of charge carriers through said superlattice

in a parallel direction relative to the stacked groups of layers; each group of layers

of said superlattice comprising less than eight stacked silicon monolayers defining

a silicon portion and an energy band-modifying layer thereon; said energy-band

modifying layer comprising a single oxygen monolayer constrained within crystal

lattice of adjacent silicon portions. "--

and all other limitations as recited in claim 46.

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V/ Group V: Claims 53-71:

None of the references of record teaches or suggests the claimed

SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE
having the limitations:

--" each group of layers of said superlattice comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon; said energy-band modifying layer comprising at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that said superlattice has a lower conductivity effective mass in the parallel direction than would otherwise be present. "--

and all other limitations as recited in claim 53.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

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Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9319 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thinh T Nguyen

David Nelms
Supervisory Patent Examiner
Technology Center 2800

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